# UNITED STATES PATENT AND TRADEMARK OFFICE

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| 10/772,349 | 02/06/2004 | Makoto Ogawa | 12377/4 | 5052 |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

| | Application No. | Applicant(s) |
| **Office Action Summary** | 10/772,349 | OGAWA ET AL. |
| | Examiner | Art Unit | |
| | Tsung-Yin Tsai | 2624 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/16/2007*.

2a)☒ This action is **FINAL**.    2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All    b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

## DETAIL ACTION

7Acknowledge of amendment received on 9/16/200 and made of record.

Acknowledge of amendment claim 1 and 6.

### *Response to Arguments*

**Applicant's argument** – Amended claims 1 and 6 as requested by Examiner to

overcome claim objections.

**Examiner's response** – Claim objections withdrawn due to amendment.

**Applicant's argument** – The Office Action indicates that every element in claims 1 and

6 of the present application is disclosed in Takahashi except "storages." In order to cure

this deficiency the Office Action cites Klein for disclosing the "storages." Further, the

Office Action indicates that claims 1 and 6 of the present application would be easily

conceived by combining Takahashi with Klein. The Applicant respectfully disagrees.

**Examiner's response** – Takahashi teaches regarding storages for the image

processing. Figure 11 discloses storages with "image memory" and "basic code size

table storing unit". Column 2 lines 20-25 discloses quantization table storing unit, as well

as column 2 lines 55-60 discloses recording apparatus to store data to prescribed

address of a recording medium. All these are see as storage.

The motivation to combine Takahashi to Klien is found in Klien's reference in column 10

lines 40-46 and column 23 lines 40-45, where cited that this format of implementation of

image processing will enable the pipelines in hardware by increasing speed with the subprocessor, allowing greater processing efficiency.

**Applicant's argument** – From the above figures and descriptions, it appears the Office Action recognizes that a "small block" and a "large block" are disclosed in claims 1 and 6 of the Applicant's claims. However, FIG. 25A is an explanation in JPEG and FIGS. 2A to 2C are explanations in the FBTC method. In other words, these figures and/or their associated descriptions do not disclose the particular relation between the "small block" formed of a plurality of pixels and the "large block" formed of the plurality of the "small blocks" as in Applicant's claims.

**Examiner's response** – Figure 2 discloses "small block" in the format of "X00, X01, X02...X33" and the "large block" is seen as the extracted 4x4 block that is compose from the element of the "small block". Figure 25 discloses the "large block" by the 8x8 pixel block, where the "large block" is compose of "small block" that are the pixel values disclose. This is the teaching from Takahashi regarding "small block" and "large block" and their relationship.

**Applicant's argument** – Further, Klein does not cure these deficiencies. Klein discloses RAM 90a-90d in FIG. 3; however, it neither teaches nor suggests a "small block" and "large block" as recited in Applicant's claims 1 and 6.

**Examiner's response** – Upon further examination Examiner discloses above regarding storage, "small block" and "large block" are taught by Takahashi, the main reference.

## *Claim Rejections – 35 USC 103*

1.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.      Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Takahashi et al (US Patent Number 6,052,488) in view of Klein et al (US Patent Number

5,029,226).

(1) Regarding claim 1:

Takahashi et al teaches the following:

An image processing device to perform image processing (figure 1

disclose a image processing device, figure 2, figure 11, figure 15, figure 20,

figure 22-24, figure 28), in which a two-dimensional image (figure 2A-2C, figure

25A-C disclose the data readout of a 2-D image, column 1 lines 50-55 disclose

image that are dealt with are of 2-D in nature) is formed of a group of pixel data

which are a matrix of plural pixel data (figure 2A-C disclose that format a image

data is read out for processing, figure 25A disclose where the image data is

output in the format of the plurality of pixel data in 8x8 matrix data block), wherein

said group of pixels are divided into small blocks (figure 2A-C disclose where the

image data is divided into small blocks, column 1 lines 45-55 disclose where the

DCT unit 61 divided the original image into a plurality of pixels blocks) formed of

a plurality of said pixel data (figure 2 disclose where the image is broken down to

plurality of pixel data, figure 25A disclose where the image is broken into matrix

of 8x8 data blocks, column 1 lines 50-55 disclose where the DCT unit 61 form the

8x8 pixel data blocks), a plurality of said small blocks form a large block (figure 2

disclose where the image is broken in the small block, where each small block is

of one pixel and form into one 8x8 large data blocks, figure 25A disclose how the

image data matrix looks like, column 1 lines 40-55 disclose where the JPED

encoder includes a DCT unit that form the large 8x8 data block from the

individual small data blocks), and in each of the large block each of the small

blocks is defined and arranged by certain rules (figure 2, figure 25, column 1

lines 40-65 disclose by what rule/equations that are use to divided up the image

data to the 8x8 large data blocks)

a calculator comprising a coefficient matrix (figure 13 disclose a

compression coefficient matrix, figure 15 part 36 disclose a compression

coefficient calculating unit, figure 20 part 40 disclose a compression coefficient

correcting unit, figure 22 part 40 disclose a compression coefficient correcting

unit, figure 23 part 56 disclose a compression coefficient estimating unit, figure

25B disclose a DCT coefficient matrix) in which a matrix of plural coefficients are

arranged (figure 25B-D disclose the matrix of plural coefficient that are arranged

in predetermine order), so that said plural coefficients are multiplied by each of

respectively corresponding pixel data and summed up (figure 6, figure 8, figure

18, figure 19, figure 24, figure 25 disclose how the plurality of coefficients are

factor in to the image data matrix, column 1-column 2); and wherein

said calculator multiplies each of the pixel data in each of said small

blocks forming said one large block, by said coefficient matrix rearranged in to a

predetermined order (figure 2, figure 6, figure 8, figure 13, figure 25 disclose pixel

data of the 8x8 block is factor in with the coefficient matrix of DCT and

Quantization table, column 2 lines 1-67 disclose the interaction of the image data

matrix to different kind of coefficient matrix such as quantization table and

Huffman coding method);

plurality of storages (Figure 11 discloses storages with "image memory"

and "basic code size table storing unit". Column 2 lines 20-25 discloses

quantization table storing unit, as well as column 2 lines 55-60 discloses

recording apparatus to store data to prescribed address of a recording medium.

All these are see as storage), small block and large block (Figure 2 discloses

"small block" in the format of "X00, X01, X02...X33" and the "large block" is seen

as the extracted 4x4 block that is compose from the element of the "small block".

Figure 25 discloses the "large block" by the 8x8 pixel block, where the "large

block" is compose of "small block" that are the pixel values disclose.  This is the

teaching from Takahashi regarding "small block" and "large block" and their

relationship).

Takahashi et al does not teaches the following:

specifying an address assigned to each small block, a plurality of pixel

data in a pertinent small block is simultaneously read out.

However, Klein et al teaches the following subject matter:

specifying an address assigned to each small block (figure 50 part 102

disclose an address generator, column 5 lines 15-50 disclose the address

generator connected to the RAM module, column 6 lines 35-68 disclose where

the address generator begin generating address for each line of image data

pixel), a plurality of pixel data in a pertinent small block is simultaneously read

out (column 5 lines 35-68 to column 6 lines 1-35 disclose how the plurality of

pixel data in memory can be signal to be read out).

It would have been obvious to one skill in the art at the time of the

invention to employ Klein et al teachings to Takahashi et al regarding a plurality

of storages, in which each of said small blocks located according to said rules

forming each of said large blocks has said pixel data independently, and by

specifying an address assigned to each small block, a plurality of pixel data in a

pertinent small block is simultaneously read out. The motivation for combination

is such that this format of implementation of the pipelines in hardware will

increase the speed associated with subprocessor (column 10 lines 40-46) and

allows for greater processing efficiency (column 23 lines 40-45).

(2) Regarding claim 2:

Takahashi et al further teaches an coefficient storage section (figure 1 part

9 disclose the coefficient estimating unit, figure 5 part 9, figure 11 part 30-31,

figure 13 is the coefficient table, column 4 lines 55-60 disclose code of figure 13

store in figure 11 storage section, column 2 lines 20-30 disclose quantization

table storing unit, column 2 lines 25-60 disclose where the estimated

compression coefficient are transferred to recording apparatus 57 and stored at a

prescribed address of a recording medium) to store said matrix coefficient

specified, an coefficient matrix converting section (figure 25A-D disclose the

image data 8x8 block are converted with/to coefficient by the DCT and

Quantization table, column 1 lines 45-56 disclose the DCT regarding the image

data block, column 2 lines 4-10 regarding the Quantizing table regarding to DCT

data matrix and the Huffman encoding method for coefficient matrix converting)

to rearrange the coefficient matrix into a predetermined order (figure 25A-D,

column 1 lines 45-56 disclose the DCT that extract the image data 8x8 block by

an equation) and correspond them to the pixel data, and an adding section to

obtain a sum of the pixel data (figure 6-9, figure 15 part 32, column 8 lines 55-67,

column 9 lines 1-15, column 10 lines 30-35), the pixel data being multiplied by

the coefficients (figure 6, figure 8, figure 18, figure 19, figure 24, figure 25

disclose how the plurality of coefficients are factor in to the image data matrix,

column 1-column 2).

(3) Regarding claim 3:

    Takahashi et al teaches adding section (figure 6-9, figure 15 part 32,

column 8 lines 55-67, column 9 lines 1-15, column 10 lines 30-35)

Takahashi et al does not teach provided for each of said storages in a

neighborhood of each of the storage, and each added result of each adding

section is independently transferred.

However, Klein et al teaches the following subject matter:

said storages in a neighborhood of each of the storage (figure 50 parts

90a-d disclose where the storage RAM modules are close to each other from the

design of the circuit), and each added result of each adding section is

independently transferred (column 5 lines 15-35, column 5 lines 35-50, column 6

lines 37-67, column 7 lines 1-30 disclose the input/output controller that request

or transfer data from between the register after processing to and from the

memories).

It would have been obvious to one skill in the art at the time of the

invention to employ Klein et al teachings to Takahashi et al regarding storages in

a neighborhood of each of the storage, and each added result of each adding

section is independently transferred. The motivation for combination is such that

this format of implementation of the pipelines in hardware will increase the speed

associated with subprocessor (column 10 lines 40-46) and allows for greater

processing efficiency (column 23 lines 40-45).

(4) Regarding claim 4 and 7:

Takahashi et al further teaches said small block is formed of said pixel

data of $m_1 \times m_2$ (figure 2 disclose where the small block is 1x1),

said large block is formed of the small blocks of $1_1 \times 1_2$ (figure 2

disclose where the large block is that of figure 2B compose of 8x8 of small data

block), said coefficient matrix is formed of said coefficients of

n.sub.1.times.n.sub.2 (figure 2, figure 25A-D disclose where the data extract to

matrix of 8x8 coefficient matrix), and the following equations are fulfilled:

n.sub.1.ltoreq.m.sub.1(1.sub.1-1)+1 and n.sub.2.ltoreq.m.sub.2 (1.sub.2-1)+1

(these standard JPEG data blocks and matrix are in accord of standard of JPEG

image encoding).

(5) Regarding claim 5:

Takahashi et al teaches regarding small block forming one large block

(figure 2 disclose where the image is broken in the small block, where each small

block is of one pixel and form into one 8x8 large data blocks, figure 25A disclose

how the image data matrix looks like, column 1 lines 40-55 disclose where the

JPED encoder includes a DCT unit that form the large 8x8 data block from the

individual small data blocks), coefficient matrix (figure 13 disclose a compression

coefficient matrix, figure 15 part 36 disclose a compression coefficient calculating

unit, figure 20 part 40 disclose a compression coefficient correcting unit, figure 22

part 40 disclose a compression coefficient correcting unit, figure 23 part 56

disclose a compression coefficient estimating unit, figure 25B disclose a DCT

coefficient matrix) and rearrangement performed to each of said coefficient

matrix (figure 2, figure 6, figure 8, figure 13, figure 25 disclose pixel data of the

8x8 block is factor in with the coefficient matrix of DCT and Quantization table,

column 2 lines 1-67 disclose the interaction of the image data matrix to different

kind of coefficient matrix such as quantization table and Huffman coding

method), said coefficient matrix is shifted by said calculator (column 2 lines 4-26

disclose where the Quantizing unit, which is seen as a form of calculator, that will

reorganize the table by the coefficient), and a plurality of said sums are obtained

(figure 2 disclose where the matrix data of image is compressed which is seen as

sum of data, figure 6, figure 8 disclose a summing function, column 8 lines 60-67

disclose an adder 16, column 9 lines 5-10 disclose adder 16 is apply to the

compression coefficient, which is sum of the image data matrix) corresponding to

each of said rearrangement performed to each of said coefficient matrix (figure 2,

figure 6, figure 8, figure 13, figure 25 disclose pixel data of the 8x8 block is factor

in with the coefficient matrix of DCT and Quantization table, column 2 lines 1-67

disclose the interaction of the image data matrix to different kind of coefficient

matrix such as quantization table and Huffman coding method).

Takahashi et al does not teach regarding specifying each address of each

of said small block forming said one large block, said not causing modification of

pertinent addresses of the small blocks.

However, Klein et al teaches the following subject matter:

specifying each address of each of said small block forming said one large

block (figure 50 part 102 disclose an address generator, column 5 lines 15-50

disclose the address generator connected to the RAM module, column 6 lines

35-68 disclose where the address generator begin generating address for each

line of image data pixel), not causing modification of pertinent addresses of the

small blocks (column 5 lines 35-67 to column 6 lines 1-67 disclose where the

data are out put for processing by subprocessor and reinsert back to memory

with address by the address generator).

It would have been obvious to one skill in the art at the time of the

invention to employ Klein et al teachings to Takahashi et al regarding specifying

each address of each of said small block forming said one large block, said not

causing modification of pertinent addresses of the small blocks. The motivation

for combination is such that this format of implementation of the same addressing

for data and pipelines in hardware will increase the speed associated with

subprocessor (column 10 lines 40-46) access to the data and allows for greater

processing efficiency (column 23 lines 40-45) due to the reduction of steps

searching for new addresses on process data.

(6) Regarding claim 6:

Takahashi et al teaches the following subject matter:

in which a two-dimensional image (figure 2A-2C, figure 25A-C disclose the

data readout of a 2-D image, column 1 lines 50-55 disclose image that are dealt

with are of 2-D in nature) is formed of a group of pixel data which are a matrix of

plural pixel data (figure 2A-C disclose that format a image data is read out for

processing, figure 25A disclose where the image data is output in the format of

the plurality of pixel data in 8x8 matrix data block), wherein:

said group of pixel data are divided into a plurality of small blocks (figure

2A-C disclose where the image data is divided into small blocks, column 1 lines

45-55 disclose where the DCT unit 61 divided the original image into a plurality of

pixels blocks) formed of said pixel data (figure 2 disclose where the image is

broken down to plurality of pixel data, figure 25A disclose where the image is

broken into matrix of 8x8 data blocks, column 1 lines 50-55 disclose where the

DCT unit 61 form the 8x8 pixel data blocks), a plurality of small blocks further

form a large block (figure 2 disclose where the image is broken in the small

block, where each small block is of one pixel and form into one 8x8 large data

blocks, figure 25A disclose how the image data matrix looks like, column 1 lines

40-55 disclose where the JPED encoder includes a DCT unit that form the large

8x8 data block from the individual small data blocks), in each of which each small

block is defined and arranged by certain rules (figure 2, figure 25, column 1 lines

40-65 disclose by what rule/equations that are use to divided up the image data

to the 8x8 large data blocks), and a plurality of coefficients are arranged in the

form of matrix to form a coefficient matrix (figure 25B-D disclose the matrix of

plural coefficient that are arranged in predetermine order);

are multiplied by said coefficients rearranged into a predetermined order

and summed up (figure 6, figure 8, figure 18, figure 19, figure 24, figure 25

disclose how the plurality of coefficients are factor in to the image data matrix,

column 1-column 2).

Takahashi et al does not teach the following subject:

each of said small blocks located according to said rules forming each of

said large blocks stores pixel data independently in each storage, and by

specifying an address assigned to each small block, a plurality of pixel data in a pertinent small block is simultaneously read, said respective pixel data of each of the small block forming said one large block, which are read out from a plurality of said storage.

However, Klein et al teaches the following subject matter:

each of said small blocks located according to said rules forming each of said large blocks stores pixel data independently in each storage (figure 50, column 3 lines 50-55 disclose the storage modules, column 4 lines 15-20 disclose the RAM/storage units, column 5 lines 15-36 disclose where the RAM contain a storage capacity of approximately one column of image data), and by specifying an address assigned to each small block (figure 50 part 102 disclose an address generator, column 5 lines 15-50 disclose the address generator connected to the RAM module, column 6 lines 35-68 disclose where the address generator begin generating address for each line of image data pixel), a plurality of pixel data in a pertinent small block is simultaneously read (column 5 lines 35-68 to column 6 lines 1-35 disclose how the plurality of pixel data in memory can be signal to be read out) out from said storage; and

said respective pixel data of each of the small block forming said one large block, which are read out from a plurality of said storage (figure 50 disclose RAM memory storage from 90a-d).

It would have been obvious to one skill in the art at the time of the invention to employ Klein et al teachings to Takahashi et al regarding each of

said small blocks located according to said rules forming each of said large

blocks stores pixel data independently in each storage, and by specifying an

address assigned to each small block, a plurality of pixel data in a pertinent small

block is simultaneously read, said respective pixel data of each of the small block

forming said one large block, which are read out from a plurality of said storage.

The motivation for combination is such that this format of implementation of the

pipelines in hardware will increase the speed associated with subprocessor

(column 10 lines 40-46) and allows for greater processing efficiency (column 23

lines 40-45).

(7) Regarding claim 8:

Takahashi et al teaches the following:

coefficient matrix is shifted by said calculator (column 2 lines 4-26 disclose

where the Quantizing unit, which is seen as a form of calculator, that will

reorganize the table by the coefficient)

and a plurality of said sums are obtained (figure 2 disclose where the

matrix data of image is compressed which is seen as sum of data, figure 6, figure

8 disclose a summing function, column 8 lines 60-67 disclose an adder 16,

column 9 lines 5-10 disclose adder 16 is apply to the compression coefficient,

which is sum of the image data matrix) corresponding to each of said

rearrangement performed to each of said coefficient matrix (figure 2, figure 6,

figure 8, figure 13, figure 25 disclose pixel data of the 8x8 block is factor in with

the coefficient matrix of DCT and Quantization table, column 2 lines 1-67

disclose the interaction of the image data matrix to different kind of coefficient

matrix such as quantization table and Huffman coding method).

Takahashi et al does not teach the following:

by specifying each address of each of said small block forming said one

large block, not causing modification of pertinent addresses of the small blocks

However, Klein et al teaches the following subject matter:

specifying each address of each of said small block forming said one large

block (figure 50 part 102 disclose an address generator, column 5 lines 15-50

disclose the address generator connected to the RAM module, column 6 lines

35-68 disclose where the address generator begin generating address for each

line of image data pixel), not causing modification of pertinent addresses of the

small blocks (column 5 lines 35-67 to column 6 lines 1-67 disclose where the

data are out put for processing by subprocessor and reinsert back to memory

with address by the address generator).

It would have been obvious to one skill in the art at the time of the

invention to employ Klein et al teachings to Takahashi et al regarding specifying

each address of each of said small block forming said one large block, said not

causing modification of pertinent addresses of the small blocks. The motivation

for combination is such that this format of implementation of the same addressing

for data and pipelines in hardware will increase the speed associated with

subprocessor (column 10 lines 40-46) access to the data and allows for greater

processing efficiency (column 23 lines 40-45) due to the reduction of steps

searching for new addresses on process data.

### Examiner's Note

Examiner requests the applicant to be more precise in the claim language to involve the

novelty of the invention.

### Conclusion

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy

as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

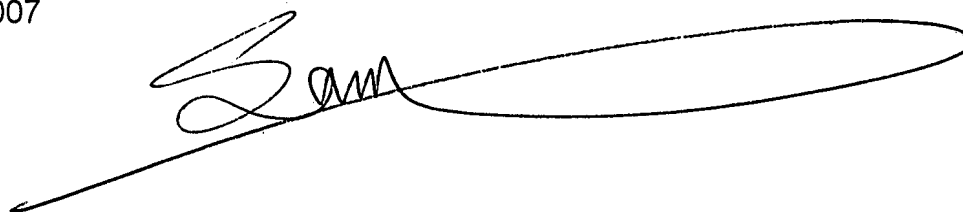than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tsung-Yin Tsai whose telephone number is (571) 270-

1671. The examiner can normally be reached on Monday - Friday  8 am - 5 pm ESP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on (571)272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tsung-Yin Tsai
September 19, 2007

SAMIR AHMED
PRIMARY EXAMINER